

10914 U.S. PTO  
09/672650  
09/26/00

	Subclass	
	Class	ISSUE CLASSIFICATION

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PATENT NUMBER

## U.S. UTILITY Patent Application

JC 2	O.I.P.E.	PATENT DATE
JCPH	SCANNED <i>as per</i> Q.A. <i>WT</i>	

APPLICATION NO. 09/672650	CONT/PRIOR	CLASS <del>711</del> <del>714</del>	SUBCLASS <del>714</del>	ART UNIT <del>2187</del>	EXAMINER <i>chase</i>
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2133  
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TITLE  
Memory tester has memory sets configurable for use as error catch RAM, tag RAM's, buffer memories and stimulus log RAM

PTO-2040  
12/99

ISSUING CLASSIFICATION					
ORIGINAL		CROSS REFERENCE(S)			
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
INTERNATIONAL CLASSIFICATION					
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TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date) _____			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____	(Primary Examiner) _____ (Date) _____			ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	(Legal Instruments Examiner) _____ (Date) _____			ISSUE BATCH NUMBER	

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